3.5 V OPERATION DRIVER-AMPLIFIER MMIC UTILIZING $SrTiO_3$ CAPACITORS FOR 1.95 GHz WIDE-BAND CDMA CELLULAR PHONES

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ABSTRUCT

This paper describes 1.95 GHz Wide-band Code Division Multiple Access power performance of a two-stage driver amplifier MMIC with 1.0 × 1.5 mm^2 area, in which double-doped AlGaAs/InGaAs/AlGaAs FETs and $SrTiO_3$ capacitors are utilized. Operated at 3.5 V with gate bias conditions chosen to reduce distortion, the complete MMIC delivered an adjacent channel leakage power ratio (ACPR) of -47.3 dBc at 5 MHz off-center frequency and an output power (P_{out}) of 73 mW (18.6 dBm) with a power-added efficiency (PAE) of 11.1 % and an associated gain of 23.5 dB. A maximum PAE of 33.2 % was obtained with P_{out} of 113 mW (20.5 dBm) at ACPR of -42.0 dBc.

INTRODUCTION

Much attention has been paid to Wide-band Code Division Multiple Access (W-CDMA) cellular systems as candidates for next generation cellular phones to further increase data stream rate and to expand system capacity [1]. To reduce size and weight of the handsets, low voltage operation with a small-sized power amplifier is a key issue. Though a few power amplifier MMICs have been reported for IS-95 CDMA systems [2], a power amplifier MMIC for W-CDMA has not been reported yet. The W-CDMA system requires lower distortion characteristics as compared to the IS-95 system due to the broadness of the carrier signal. This paper is the first report of an amplifier MMIC for W-CDMA wireless communication systems. A low adjacent channel leakage power ratio (ACPR) of -47.3 dBc at 5 MHz off-center frequency with 4.096 MHz band width and a high power added efficiency (PAE) of 33.2 % were attained under 3.5 V operation.

DESIGN AND FABRICATION

The MMIC is a two-stage amplifier with double-doped AlGaAs/InGaAs/AlGaAs FETs (HJFET), $SrTiO_3$ (STO) capacitors and spiral inductors. A 6 μm-thick plated gold layer was employed for interconnections and for the spiral inductors to reduce DC and RF loss. A plated heat sink was formed on the back side of the wafer after thinning, to ensure low thermal resistance.

Figure 1 shows the HJFET structure. A double recessed structure, fabricated by dry-etching, yielded a threshold voltage of -0.8 V with a 20 mV standard deviation on a 3 inch wafer. The fabricated 1.0 μm gate-length HJFET exhibited a maximum drain current of 560 mA/mm with a gate-to-drain breakdown voltage of 16 V. It has a low on-resistance of

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2.3 Ωmm, which is noteworthy as favorable for high efficiency with low distortion [3].

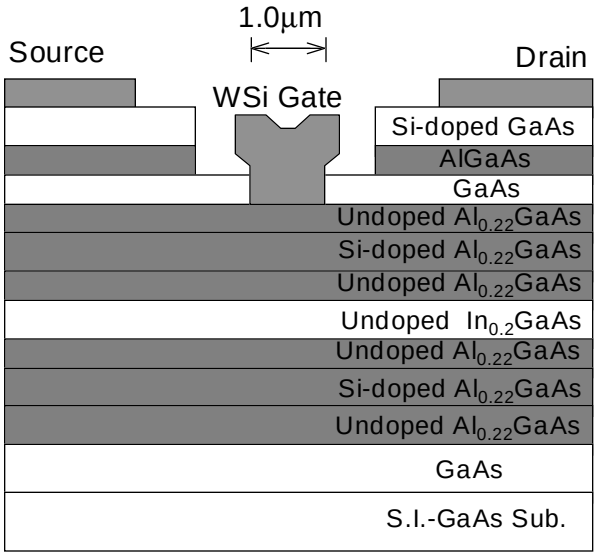

Figure 1: Cross section of the HJFET

Figure 2 shows the STO capacitor structure. An STO film was deposited by an RF-sputtering method at a substrate temperature of 400 °C. This low temperature process is expected to reduce possible thermal damage to the epitaxial layers of the HJFET as compared to a previously reported one[4]. The capacitor exhibited a high relative dielectric constant (ε_r) of 160, resulting in substantial reduction in the matching and bias circuit areas.

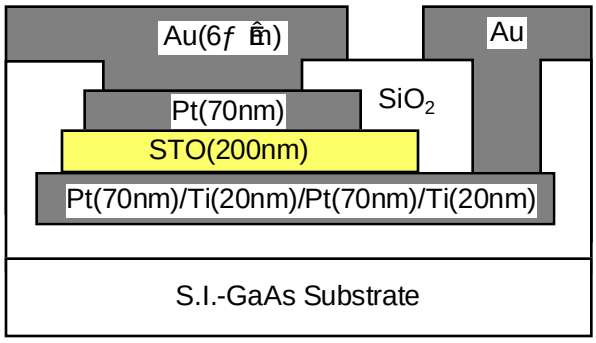

Figure 2: Cross section of the STO capacitor

Figure 3 shows the circuit configuration of the two-stage amplifier MMIC. The gate width for the first and second stage HJFETs are 0.5 and 2.0 mm, respectively. The amplifier includes all matching and bias circuits for both FETs. Harmonic suppression circuits were employed in the bias circuits.

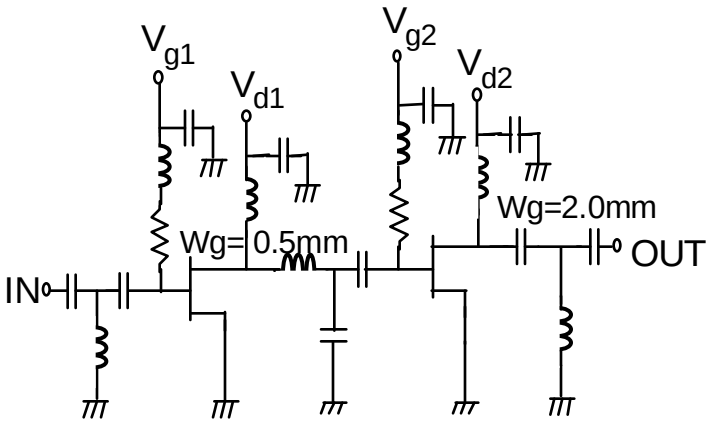

Figure 3: Circuit configuration of the MMIC

Figure 4 shows a microphotograph of the MMIC. The chip size is 1.0 × 1.5 mm^2. High power density of the HJFET and high ε_r of the STO capacitor resulted in substantial reduction in the size of MMIC.

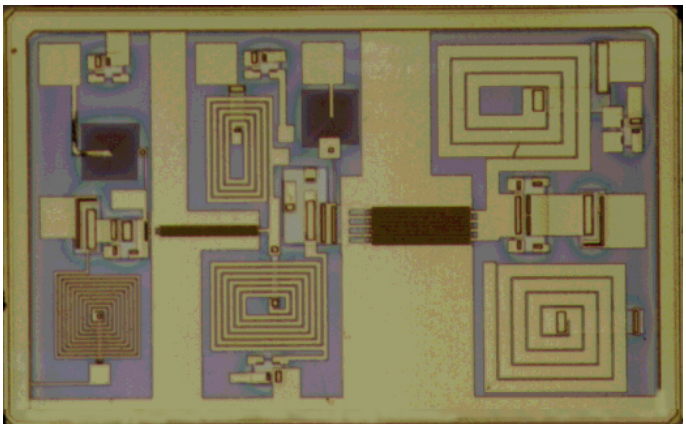

Figure 4: Microphotograph of the MMIC
(Chip Size: 1.0×1.5 mm^2)

RESULTS AND DISCUSSION

1.95 GHz power performance of the MMIC was evaluated at a drain bias voltage (V_d) of 3.5 V. For a cellular phone application in which 300 mW RF output power is required [1], the MMIC would be utilized as a driver amplifier for a final power stage. Assuming a final power stage with ACPR lower than -43 dBc, the required ACPR of the driver amplifier MMIC was estimated to be lower than -47 dBc. The optimum gate bias conditions were determined to be a quiescent drain current of the first-stage FET(I_{q1}) of 55 mA and that of the second-stage FET (I_{q2}) of 120 mA. Figure 5 shows the power performance of the MMIC.

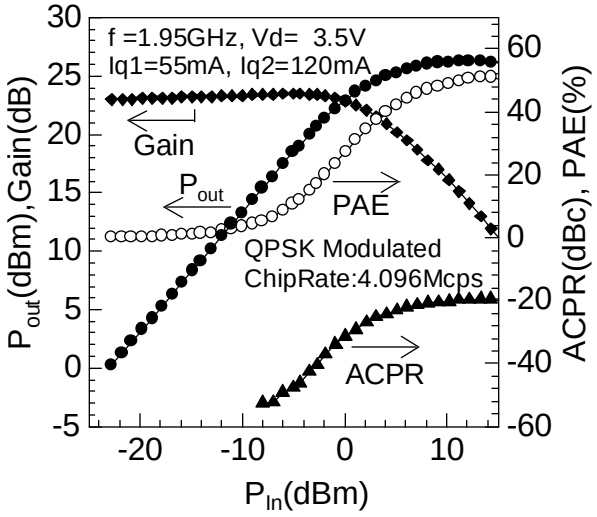

Figure 5: P_{out}, PAE, gain and ACPR vs. P_{in}

The MMIC exhibited a low ACPR of -47.3 dBc and an output power (P_{out}) of 73 mW (18.6 dBm) with PAE of 11.1 % and an associated gain (G_a) of 23.5 dB. Figure 6 shows the P_{out} and PAE as a function of I_{q2} at several ACPRs. The maximum PAE was obtained at I_{q2} = 120 mA while the P_{out} increased with the increase of I_{q2}.

For a final amplifier application of indoor use, in which 20 mW RF output power is required [1], the MMIC would be utilized as a power amplifier with no subsequent amplifying stage. The I_q dependence of W-CDMA power performance was evaluated in order to achieve high PAE. Figure 7 shows PAE and ACPR as a function of P_{out} for the MMIC with various I_{qs} at V_d of 3.5 V. For the typical P_{out} of 40 mW, PAE of 10.9 % was obtained at I_{q1} = 10 mA and I_{q2} = 75 mA.

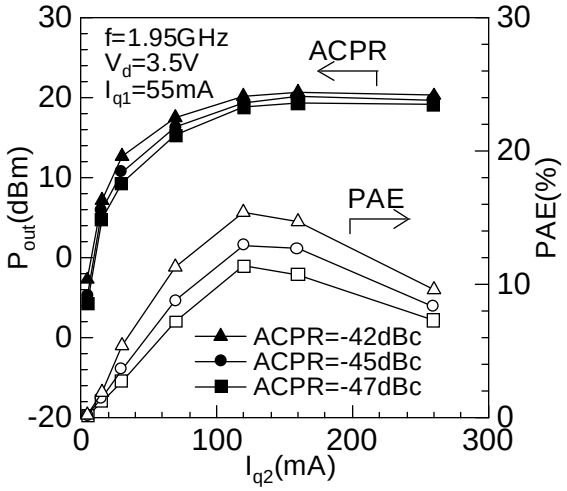

Figure 6: P_{out} and PAE vs. I_{q2}.

A maximum PAE of 33.2 % with P_{out} of 113 mW (20.5 dBm) was obtained with ACPR of -42.0 dBc at I_{q1} = 10 mA and I_{q2} = 10 mA.

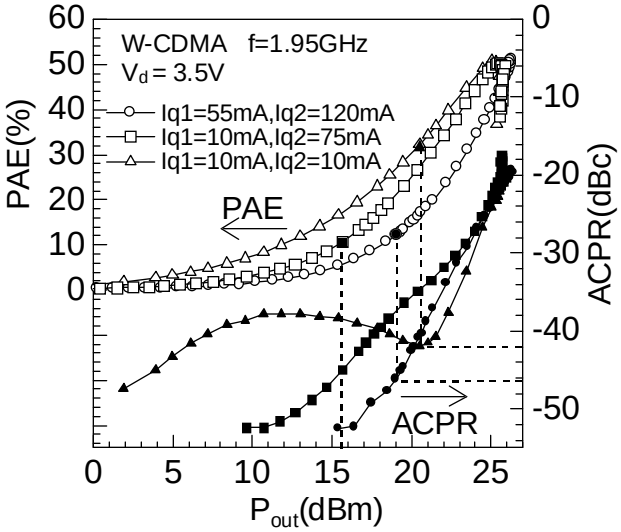

Figure 7: PAE and ACPR vs. P_{out} for the MMIC

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These results indicate that the developed MMIC has great potential as a driver amplifier for cellular phones and as a power amplifier for indoor use, which can be operated with one Li-ion battery cell.

CONCLUSION

A two-stage driver amplifier MMIC utilizing double-doped AlGaAs/InGaAs/ AlGaAs HJFETs and STO capacitors with 1.0 × 1.5 mm^2 area was successfully developed for 1.95 GHz Wide-band CDMA applications. Operated at 3.5 V with gate bias conditions chosen to reduce distortion, the complete MMIC delivered an ACPR of -47.3 dBc and P_{out} of 73 mW (18.6 dBm) with PAE of 11.1 % and G_a of 23.5 dB. For the typical indoor use P_{out} of 40 mW, PAE of 10.9 % was obtained. A maximum PAE of as high as 33.2 % was obtained with P_{out} of 113 mW (20.5 dBm) at ACPR of -42.0 dBc.

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